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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Response to Arguments

1. Examiner as accepted Applicant's new drawing (6/10/2009) and the corresponding change in the specification.

2. Applicant's arguments filed 6/10/2009 have been fully considered but they are not persuasive.

Argument: Applicant argued that (a) Medlock does not disclose carrying out word-based, hard-wired operations to process first and second words in order to obtain a correlation value (Remarks 6/10/2009, page 9, last paragraph, 2nd line onwards) (b) that Medlock disclosed that the correlation process is implemented one chip at a time (Remarks 6/10/2009, page 9, last paragraph, 5th line onwards) and that (c) processing two separate signals in parallel on a bit-by-bit basis is not the same as word-based processing because the separate chips or bits from separate signals do not constitute a word, even if they are processed in parallel.

Response: Examiner respectfully disagrees. Medlock states that in Fig. 3, multiply block 304 contains multiple multiply logic devices in the present embodiment for multiplying chips of a first code sequence with chips of a second code sequence then summing them with an adder [0043], lines 8 – 11). Medlock then clearly states that in one embodiment, the multiply circuit has bit slices that contain a multiply-logic device for parallel correlating operations on a chip-by-chip basis. This clearly differentiates from the previous embodiment since Medlock states that that parallel correlating is used. In parallel correlating it is well known that the multiply operations are performed in parallel and opposed to sequentially, since this speed ups the correlation process at the

expense of more hardware. The chips are parallel are interpreted as one bit values combined to form a word. This interpretation is consistent with what he Applicant has described in his specification as to how a word is formed (see Specification, page 2, lines 23- 28). Therefore, Examiner respectfully disagrees with Applicant's statement that that Medlock does not disclose word based processing and also does not disclose that the multiplication process is performed in parallel.

/Adolf DSouza/
Examiner, Art Unit 2611

/Mohammad H Ghayour/
Supervisory Patent Examiner, Art Unit 2611